(12) PATENT APPLICATION PUBLICATION
(19) INDIA
(22) Date of filing of Application :30/08/2022

(21) Application No.202211049364 A
(43) Publication Date : 02/09/2022

(54) Title of the invention : DESIGN AND IMPLEMENTATION OF LOW POWER MULTIPLIERS USING POWER EFFICIENT ADDER BLOCKS

(51) International classification	:G06K0007100000, B29C0065180000, G06T0005500000, G06Q0030020000, A61K0048000000
(86) International Application No Filing Date	:NA :NA
(87) International Publication No	: NA
(61) Patent of Addition to Application Number Filing Date	:NA :NA
(62) Divisional to Application Number Filing Date	:NA :NA

(71)**Name of Applicant :**
1)Debika Chaudhuri
Address of Applicant :Assistant Professor, ECE Department, School of Engineering & Technology, IFTM University, Moradabad, U.P-244102, India Moradabad ---------- ----------
2)Dr. Atanu Nag
3)Dr. Shalu C.
Name of Applicant : NA
Address of Applicant : NA
(72)**Name of Inventor :**
1)Debika Chaudhuri
Address of Applicant :Assistant Professor, ECE Department, School of Engineering & Technology, IFTM University, Moradabad, U.P-244102, India Moradabad ---------- ----------
2)Dr. Atanu Nag
Address of Applicant :Associate Professor, Department of Physics, School of Sciences, IFTM University, Moradabad, U.P-244102, India Moradabad ---------- ----------
3)Dr. Shalu C.
Address of Applicant :Assistant Professor, ECE Department, School of Engineering & Technology, IFTM University, Moradabad, U.P-244102, India Moradabad ---------- ----------

(57) Abstract :
The invention relates to design and implementation of low power multipliers using power efficient adder blocks. The design of digital multipliers is very common and already many such designs for low power digital multiplier have been proposed. The multiplier block is designed using Tanner tool 180 nm Complementary Metal Oxide Semiconductor (CMOS) technology. In this paper, an attempt has been made to optimize the performance of an array multiplier which consumes low power. The multiplier has been designed and simulated by using various adder blocks. The work includes the design of basic gates, half adder and full adder, operated with different operating voltages. The used logic styles in our proposed CMOS logic design of the multiplier are 14T full adder, 16T full adder, SERF full adder, and CPL full adder and TG full adder. The power, delay analysis has been computed and compared for the different used logic styles.

No. of Pages : 27 No. of Claims : 7